**IN THE CLAIMS:**

Please amend claims 1, 27 and 29 as follows:

1 (3rd amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area;

a first dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area;

a first insulating layer formed on the circuit area and the peripheral area of the semiconductor substrate;

a second insulating layer formed on the first insulating layer which is formed on the semiconductor substrate, wherein the second insulating layer is formed over the wiring patterns, and the second insulating layer is not formed over the first dummy pattern; and

a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

27 (2nd amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is

formed and a peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area; and

an insulating layer formed above the semiconductor substrate, the insulating layer being formed over the wiring patterns, the insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern, and the insulating layer having a moisture absorbable characteristic.

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29 (2nd amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area, the wiring pattern including a pad pattern;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area;

a first insulating layer formed over the wiring patterns and the dummy pattern, an edge of the first insulating layer being located on the pad pattern, which is adjacent the dummy pattern; and

a second insulating layer formed above the semiconductor substrate, the second insulating layer being formed over the wiring patterns and the second